This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-6 (canceled).

7 (currently amended). ~~The method of claim 1,~~ A method of clearing obsolete entries from a first one of a plurality of mapping caches, each of the plurality of mapping caches being associated with a corresponding one of a plurality of processing units of a computing device, each of the caches being used to translate virtual addresses to physical addresses and storing mappings based on an address translation map, the method comprising:

maintaining a counter;

updating said counter each time the first one of the plurality of mapping caches is flushed;

recording said counter's value in response to a change in the address translation map, whereby a recorded counter value is stored;

determining, based on a comparison of said counter's value with the recorded counter value, that the first one of the plurality of mapping caches has not definitely been flushed since said change in the address translation map occurred; and

flushing the first one of the plurality of mapping caches;

wherein a policy defines permissible access to a memory, and wherein the method further comprises:

controlling the content of the address translation map such that the address translation map does not expose to an entity virtual address mappings that would permit said entity to access said memory in violation of said policy;

wherein said change comprises either a modification to the map that places or maintains the map in conformance with said policy, or a modification to the map that limits said entity's write access to the map.

8 (original). The method of claim 7, wherein the address translation map comprises a link to a portion of said memory, wherein controlling the content of the address translation map comprises making said portion of said memory inaccessible to said entity, and wherein

said change comprises removing all links to said portion of said memory from the address translation map.

9-10 (canceled).

11 (currently amended). A system for managing the use of address mapping caches, the system comprising:

a plurality of processors, each of the processors having a mapping cache and a counter associated therewith;

a memory that stores an address translation map, each of the mapping caches storing mappings based on said address translation map, there being a policy that governs access to said memory, the contents of the address translation map being controlled to prevent exposure of mappings that permit access to said memory in violation of said policy;

first logic that flushes a first one of the mapping caches and that increments a first one of the counters when said first one of the mapping caches is flushed;

second logic that records the ~~current~~ value of said first counter in response to a change in said address translation map or in a property regarding said address translation map, the recorded counter value being stored in association with said change;

third logic that compares the recorded counter value with the current value of the first counter and that causes said first one of the mapping caches to be flushed if the comparison indicates that said first one of the mapping caches has not been flushed since the change.

12 (original). The system of claim 11, wherein each of the processors is associated with said first one of the counters, and wherein said first logic increments said first one of the counters when any of the mapping caches is flushed.

13 (original). The system of claim 11, wherein each of the mapping caches is associated with a different one of a plurality of counters, and wherein said first logic increments the counter corresponding to a given mapping cache when the given mapping cache is flushed.

14 (original). The system of claim 11, wherein said change comprises placing said address translation map in a state in which all links to a first page of said memory are removed from said address translation map.

15 (original). The system of claim 11, wherein said change comprises placing said address translation map in a state in which there is no writeable link to a first page of said memory.

16 (original). The system of claim 11, wherein said third logic is invoked in response to a detection that a result of said change is to be used.

17 (original). The system of claim 16, wherein said change comprises placing said address translation map in a state in which all links to a first page of said memory are removed from said address translation map, and wherein said detection is based on a virtual address having been translated to a location on said first page.

18-19 (canceled).

20 (currently amended). ~~The computer-readable medium of claim 18,~~ A computer-readable medium having encoded thereon computer-executable instructions to perform a method of managing the flushing of a translation lookaside buffer that caches address mappings, the method comprising:

receiving an access request that indicates a target location by virtual address;

translating said virtual address to obtain a physical address of said target location;

comparing (1) a stored counter value associated with a page that comprises said target address with (2) a current counter value;

determining based on the comparison between said stored counter value and said current counter value that the translation lookaside buffer has not been flushed since an event affecting a mapping of said page; and

flushing the translation lookaside buffer;

wherein a policy defines accessibility of a memory to a software entity, and wherein said event comprises removing links to a page of said memory from an address translation map on which said address mappings are based, said page being inaccessible to said software entity under said policy.

21 (currently amended). ~~The computer readable medium of claim 18,~~ A computer-readable medium having encoded thereon computer-executable instructions to perform a method of managing the flushing of a translation lookaside buffer that caches address mappings, the method comprising:

receiving an access request that indicates a target location by virtual address;

translating said virtual address to obtain a physical address of said target location;

comparing (1) a stored counter value associated with a page that comprises said target address with (2) a current counter value;

determining based on the comparison between said stored counter value and said current counter value that the translation lookaside buffer has not been flushed since an event affecting a mapping of said page; and

flushing the translation lookaside buffer;

wherein a policy defines accessibility of a memory to a software entity, and wherein said event comprises adjusting an address translation map to make mappings to a page non-writeable, wherein either: (1) said policy defines said page as being non-writeable by said software entity, or (2) said page stores a portion of said address translation map.

22-28 (canceled).